CLAIMS

What Is Claimed Is

1. A chip-scale package comprising:

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a memory die mounted on the first surface of the substrate using a plurality of rigid underside coupling members, the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the memory die;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to at least one of the underside coupling members;

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and

one or more electronic components mounted on the second surface of the substrate in an area substantially opposite of the memory die, wherein the combined distance that an electronic component and the memory die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

2. The chip-scale package of claim 1 further comprising:

electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die.

3. The chip-scale package of claim 1 wherein the substrate includes a controlled thermal expansion material that sufficiently matches the coefficient of expansion of the memory die.

4. The chip-scale package of claim 1 wherein the underside coupling members permit the underside surface of the memory die to be substantially exposed.

5. A chip-scale package comprising:

a substrate having a first surface and an opposite second surface;

a semiconductor device mounted on the first surface of the substrate using solder balls;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to the semiconductor device;

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and

one or more electrical components mounted on the second surface of the substrate.

6. The chip-scale package of claim 5 wherein the electrical components are mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device.

7. The chip-scale package of claim 6 wherein the electrical components include capacitors and resistors.

8. The chip-scale package of claim 5 wherein the combined distance that an electrical component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

9. The chip-scale package of claim 5 wherein the substrate includes a controlled thermal expansion material with a coefficient of expansion that substantially matches the coefficient of expansion of the semiconductor device.

10. The chip-scale package of claim 5 wherein the semiconductor device is a silicon device and the substrate includes a controlled thermal expansion material that sufficiently matches the coefficient of expansion of the silicon device.

11. The chip-scale package of claim 5 further comprising:

electrically conductive traces on the first surface to electrically couple at least one solder ball to the semiconductor device.

12. The chip-scale package of claim 5 wherein the semiconductor device is a silicon memory device.

13. The chip-scale package of claim 5 wherein the semiconductor device is coupled to the first surface using rigid underside coupling members.

14. The chip-scale package of claim 13 wherein the rigid underside coupling members permit the underside surface of the semiconductor device to be substantially exposed.

15. A stackable electronic assembly comprising:

a plurality of chip-scale packages, the plurality of chip-scale packages arranged in a stacked configuration, each chip-scale package including

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a semiconductor device coupled to traces on the first surface of the substrate using underside coupling members, the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the semiconductor device;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to the semiconductor device;

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and

one or more electrical components mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device, wherein the combined distance that an electronic component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

16. A stackable electronic assembly of claim 15 wherein the plurality chip-scale packages have identical routing traces.

17. A stackable electronic assembly of claim 15 wherein the solder balls on the first surface of a first chip-scale package are coupled to the pads on the second surface of a second chip-scale package.

18. A stackable electronic assembly of claim 15 wherein the staggered routing scheme permits accessing the same underside coupling member in each of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package.

19. The stackable electronic assembly of claim 15 wherein the underside coupling members permit the underside surface of the semiconductor device to be exposed.

20. A memory module comprising:
a main substrate with an interface to couple the memory module to other devices; and
one or more stacks of memory devices coupled to a first surface of the main substrate,
at least one stack of memory devices including
a plurality chip-scale packages, the plurality of chip-scale packages arranged in a stacked configuration and having identical routing traces on a first surface and opposite second surface of the chip-scale package, each chip-scale package including
a substrate having a first surface and an opposite second surface,
a memory semiconductor die electrically coupled to traces on the first surface of the substrate using underside coupling members, and
a plurality of solder balls mounted on the first surface of the substrate, at least one of the solder balls electrically coupled to the memory semiconductor die.

21. The memory module of claim 20 wherein
the substrate is composed of a controlled thermal expansion material,

the substrate has a coefficient of expansion that substantially matches a coefficient of expansion of the memory semiconductor die,

the plurality of solder balls are mounted on the first surface of the substrate in a ball grid array configuration, and

each chip-scale package further includes

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme, and

one or more electronic components mounted on the second surface of the substrate in an area substantially opposite of the memory semiconductor die, wherein the combined distance that an electronic component and the memory semiconductor die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

22. The memory module of claim 21 wherein the staggered routing scheme permits accessing the same underside coupling members in all of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package.

23. The memory module of claim 20 wherein the memory module is a dual inline memory module.

24. The memory module of claim 20 further comprising:

one or more stacks of memory devices coupled to a second surface of the main substrate.

25. The memory module of claim 20 wherein the chip-scale packages are stacked with the solder balls on the first surface of a chip-scale package coupled to pads on the second surface of another chip-scale package.

26. The memory module of claim 20 wherein the underside coupling members permit the underside surface of the memory semiconductor die to be exposed.